

APPLICANT(S): SHAHAR ATIR  
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#### **REMARKS**

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

#### **Status of Claims**

Claims 1-17 are pending in the application. Claims 1-11 have been rejected. Claims 12-17 have been withdrawn from consideration. Claims 1, 5, 6, 10 and 11 have been amended.

#### **CLAIM REJECTIONS**

##### **35 U.S.C. § 112 Rejections**

In the Office Action, the Examiner rejected claims 5-6 and 10-11 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

More specifically, the Examiner rejected claims 5, 6, 10 and 11, for allegedly lacking sufficient antecedent basis for the limitation "wherein said coupling a sense amplifier...". Applicant has voluntarily amended claims 5, 6, 10 and 11, so that currently they depend upon claim 2. Applicant respectfully asserts that these amendments cure the deficiency stated by the Examiner, and thus claims 5, 6, 10 and 11 are now considered allowable.

Accordingly, Applicant respectfully asserts that claims 5, 6, 10 and 11 are proper under 35 U.S.C. §112, and requests that the rejections of claims 5, 6, 10 and 11 be withdrawn.

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In addition, Examiner rejected claims 6 and 11 for allegedly reciting conflicting limitations with limitations recited in claims 1 and 2. Applicant respectfully traverses these rejections, because the Examiner seems to have misinterpreted the subject matter which Applicant regards as the invention.

More specifically, as the Examiner should know, and as recited in the Application, the NVM cells are symmetric and thus source/drain side operations are interchangeable. Furthermore, the current of non-adjacent local bit lines can be tied through a common global bit line with select transistors and the current can be fed to a common sense amplifier. In response to the Examiner's assertion that there is no support for a common sense amplifier, Applicant respectfully points that Examiner's attention to paragraph [0024] of the Specification.

Accordingly, Applicant respectfully asserts that claims 6 and 11 are proper under 35 U.S.C. §112, and requests that the rejections of claims 6 and 11 be withdrawn.

#### **35 U.S.C. § 102 Rejections**

In the Office Action, the Examiner rejected claims 1-8 and 10-11 under 35 U.S.C. § 102(b), as being anticipated by Thewes et al. (US Patent No. 5,831,892) or Park et al. (US Patent No. 4,992,980).

Applicant respectfully asserts that the Examiner has failed to establish a prima facie case of anticipation, because both cited references neither teach nor suggest every element and limitation recited in independent claim 1 as filed.

In the interest of expediting the prosecution of the present Application, however, Applicant has voluntarily amended independent claim 1 in order to better clarify the subject matter recited in the claim and to better point to the essence of the present invention.

More specifically, Applicant has amended independent claim 1, so it now includes the limitations of "...sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path including a common sense amplifier..." and "...wherein sensing includes applying a first voltage to a common word line and a

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substantially similar voltage to source side bitlines of the cells." Applicant respectfully asserts that these amendments distinguish in an even clearer fashion the subject matter recited in independent claim 1 from the teachings of each of the cited references and of any other known prior art in the field.

More specifically, amended claim 1 now recites:

1. "A method of reading data in a virtual ground array of memory cells comprising: sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path including a common sense amplifier, wherein sensing includes applying a first voltage to a common word line and a substantially similar voltage to source side bitlines of the cells."

Whereas, the Thewes reference teaches:

"Every bit line provided for the readout is connected to the drain terminals of two neighboring field effect transistors in the same row. The source terminals are applied to one of two potentials which differ from each other." (Col.1 lines 53-57)

And the Park reference teaches:

"The two adjacent column lines—one on each side of the grounded column line—are coupled to separate read paths." (Abstract lines 9-11);

"Collectively, devices 46 and 45 select the various column lines used to access pairs of memory cells within the array. The gates of each of these devices are coupled to decode circuitry (not shown) which functions to select pairs of bits to be read or programmed. By way of example, the gate of device 46c (labelled Y.sub.1,2), is raised to select n- output line 75b. Similarly, the gate of device 45b (labelled Y.sub.1) may be raised to a positive potential (e.g., 5 Volts) to connect n+ drain line 76a to line 50." (Col. 4 lines 33-42)

As shown above, after reading the pending independent claim (after amendment) and the excerpts from the cited references, it should be clear to anyone of ordinary skill in the art that both references are insufficient prior art references for the purpose of establishing a case of anticipation. Moreover, as shown, the cited references actually teach away from the limitations of "...sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path including a common sense amplifier..."

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and "...sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path, wherein sensing includes applying a first voltage to a common word line and a substantially similar voltage to source side bitlines of the cells." of amended independent claim 1.

Accordingly, Applicants respectfully assert that the Examiner's 102 rejections of claims 1-8 and 10-11 are now moot in light of the current amendment to pending independent independent claim 1.

Applicants respectfully request withdrawal of the rejections of independent claim 1 under 35 U.S.C. 102 and allowance thereof. All claims depending from independent claim 1 are also considered allowable by virtue of their dependence on an allowable base claim.

#### **35 U.S.C. § 103 Rejections**

In the Office Action, the Examiner rejected claim 9 under 35 U.S.C. § 103(a), as being unpatentable over Thewes/Park in view of Maayan et al. (US Patent No. 6,975,536).

In view of the voluntary amendment made to independent claim 1, and the aforementioned clarifying remarks, Applicant asserts that claim 9 is allowable by virtue of its dependence on an allowable base claim. Accordingly, reconsideration and withdrawal of the 103 rejection is respectfully requested.

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In view of the foregoing amendments and remarks, all the pending claims are considered to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned Attorney of Record. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to contact the undersigned Attorney of Record.

Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,



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